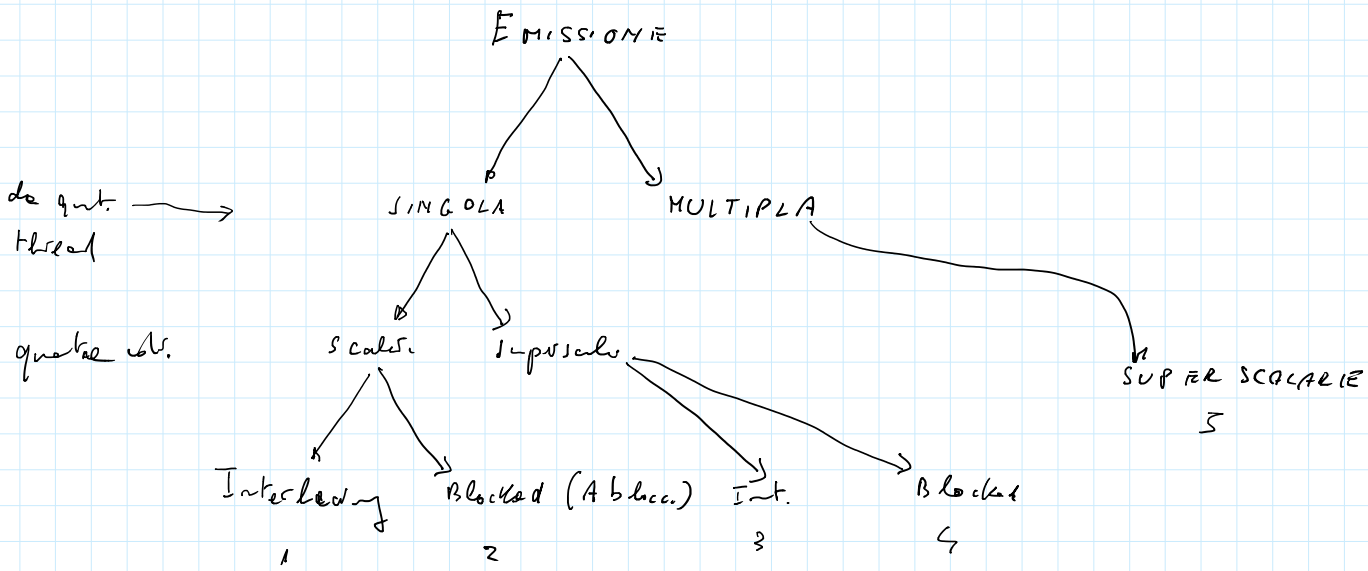
SOLUZIONI MULT. THREAD



1 Single / scalare / Interleaving

$n = 2$

T_1

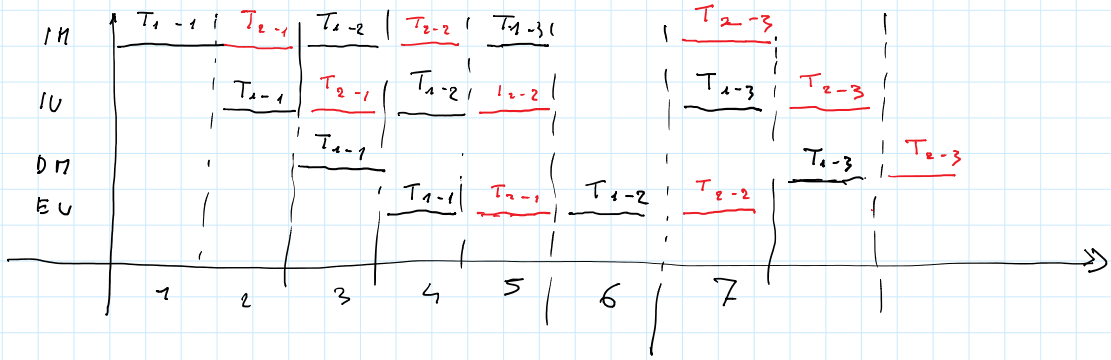
1. LD Ra Rb Rc
2. ADD Rc Rd Rc
3. ST Ra, Rb, Rc

T_2

1. MUL Ra, Rb, Rc
2. ADD Rb, Rc, Rc
3. ST Ra, Rb, Rc

6 istruzioni in 7 CC

eff. $\frac{6}{7} \simeq 0.85$

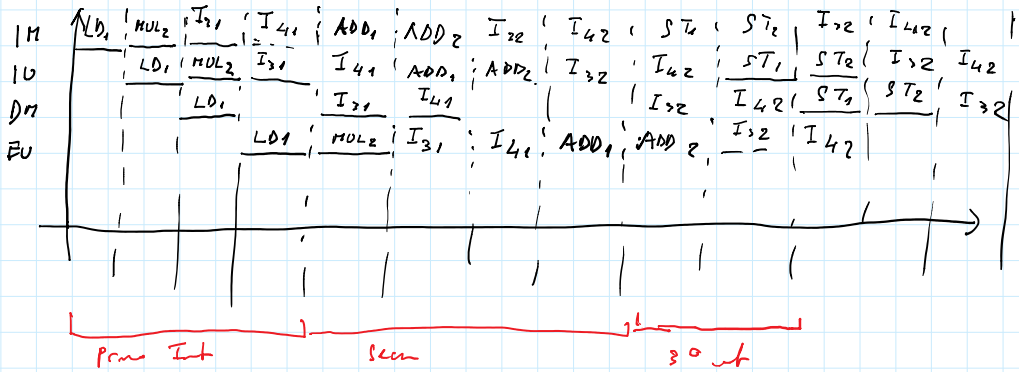


$n = 4$

T_1	T_2	T_3	T_4
LD_1	MUL_2	I_{31}	I_{41}
ADD_1	ADD_2	I_{32}	I_{42}
ST_1	ST_2	I_{33}	I_{43}

Aumentando il n° di contesti aumenta la distanza fra due istr. in esecuzione

⇒ Riduce il degrado dovuto alle dip. log.



$n = 2 \longrightarrow 0.85$

$n = 4 \longrightarrow 1$

EMISSIONE SINGOLA SCALARE BLOCKED

Switching tra contesti → Quando si incontra dipendenza

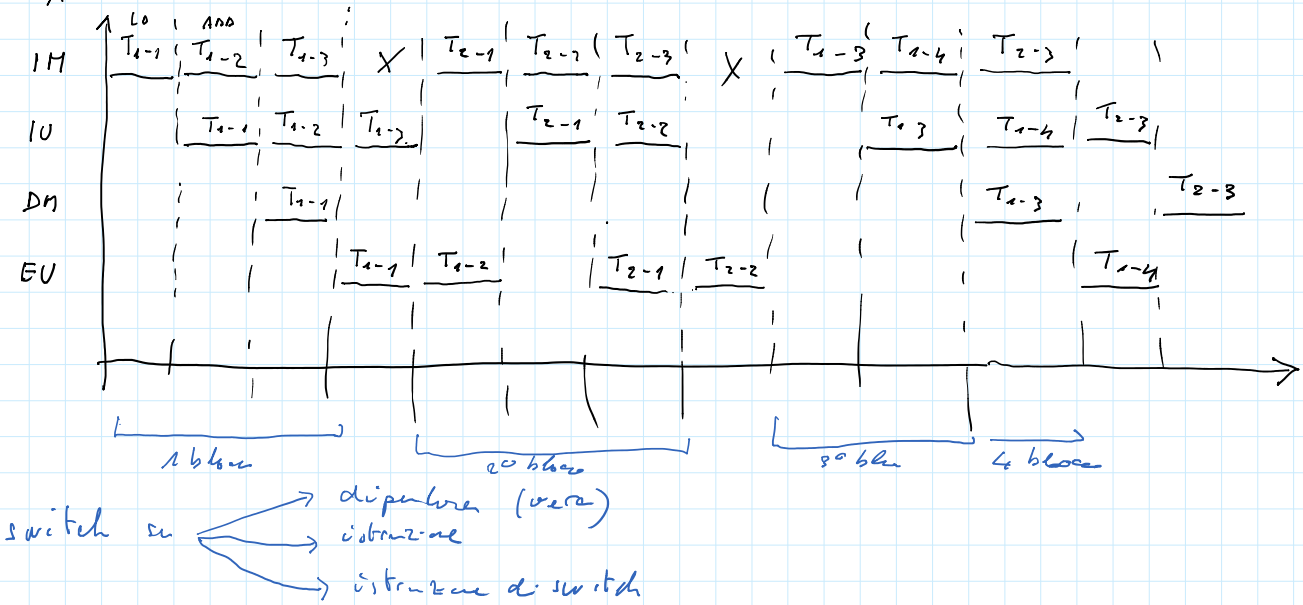
$n = 2$

T_1

LD 1
ADD 1
ST 1
ADD

T_2

MUL
ADD
ST



switch su → dipendenza (vera)
→ istruzione
→ istruzione di switch

Emissione Single Super scalare

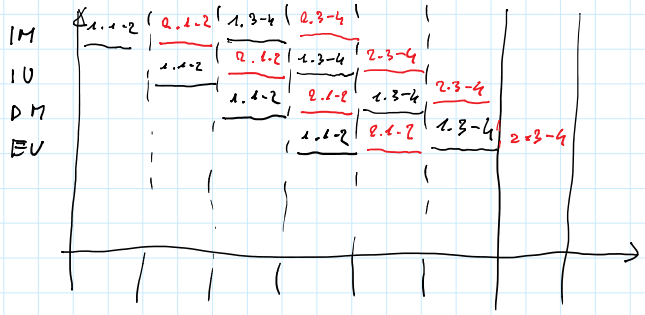
LD_1
LD_2
MUL
INC_1
ST
INC_2

→

1-2 LD_1 LD_2
3-4 MUL INC_1
5-6 ST INC_2

] T_1, T_2

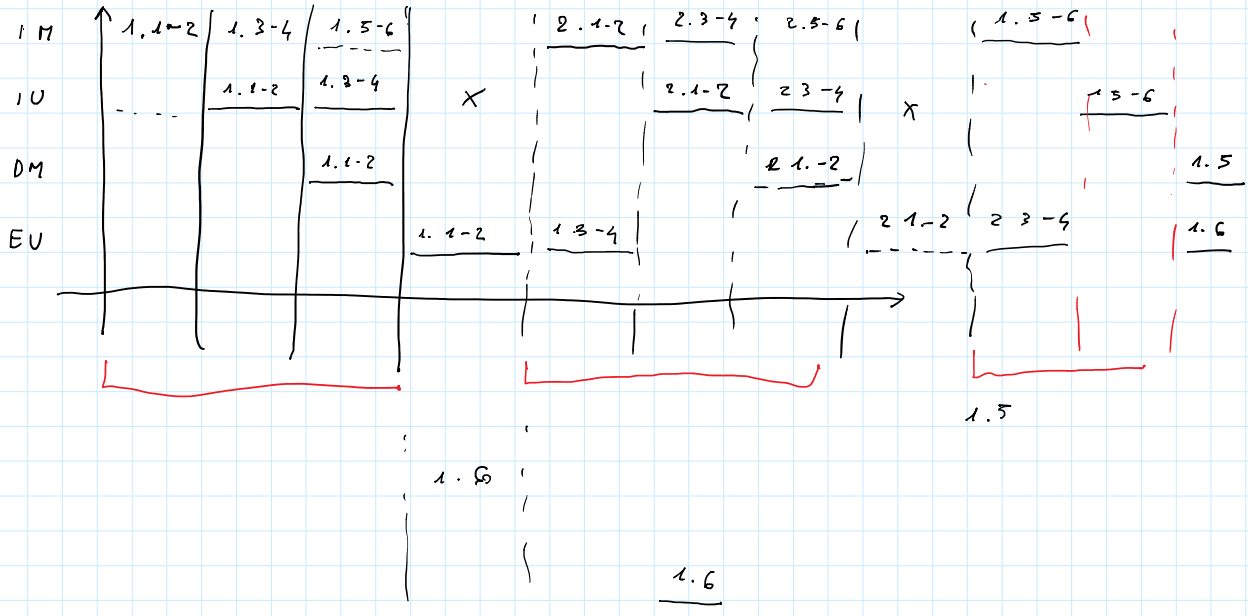
Interleaving $n=2$ 2 thread, ognuno con istruzione lunga 2



LD LD
MUL INC
ST INC

$n=2$, stesso progr. blocked

Blocked



Simultaneous MT

Emissione Multipla / Superscalare / SMT

T_1	LD	Ra	Rb	Rc
	ADD	Rc	Rd	Rc
	ADD	Rc	Rd	Rc
	MUL			
	ST			

T_2	MUL
	DIV
	ST
	ADD
	ADD

T_3	LD
	MUL
	DIV
	ADD
	ST

$n = 2$

T_1	T_2	
LD	MUL	L_1
ADD	DIV	L_2
ADD	ST	L_3
MUL	ADD	L_4
ST	ADD	L_5

T_2	T_3
MUL	LD
DIV	MUL
ST	DIV
ADD	ADD
ADD	ST

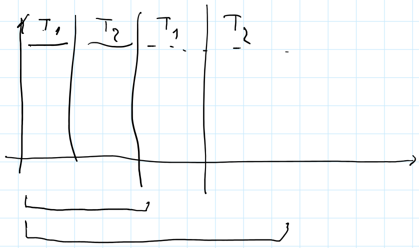
T_1	T_3
LD	LD
ADD	MUL
ADD	DIV
MUL	ADD
ST	ST

Accoppiamento Statico → All. Memoria

Accoppiamento Dinamico

⇒ Prelievo in memoria in parallelo da thread diversi

Problema → } core → acc. statici
→ } core → acc. statici



Abstract del corso

1) Comp / Interpr.

2) Gerarchia di macchine virtuali

- Firmware → D.p. unità / Cache
- Assembler

3) Istruzione LM

Istruzione AL

N Istruzione