

COPROCESSORE SLAVE

```
for { i = p, i < N, i++ } { U[i] = Z[i] * C[i] }
```

$U, Z, C \rightarrow FP$

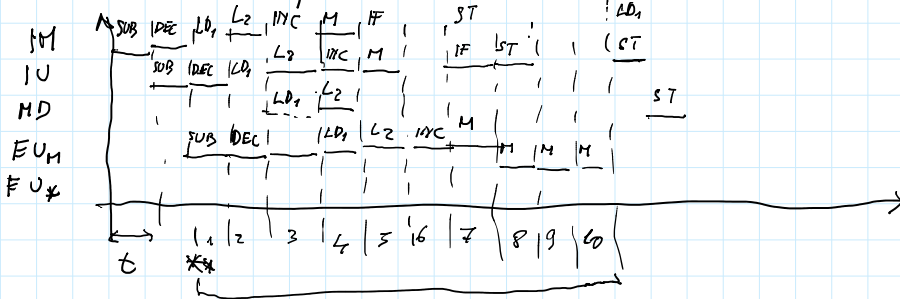
3 archit. slave per #

$R_U, R_Z, R_C \rightarrow$ indirizzi base vettore

$n \times t \times 10 \rightarrow$ reale
 $ideck \rightarrow 6 \times n \times t$ } eff. 60%

```

SUB R1, R1, R1
DEC RV
LOOP : LD, RC, R1, Rf1
      LD2, RZ, R1, Rf2
      INC R1
      MUL Rf1, Rf1, Rf1
      IFC R1, RM, LOOP ← delayed branch
      ST RV, R1, Rf1
    
```



```
for { i = p, i < N, i++ } { A[i] = B[i] + C[i];
                          D[i] = B[i] * C[i] }
```

$A-D \equiv$ iterazioni; \equiv U semplice / t

no fault B/C $\approx n/\sigma =$ in pipeline

no fault $\approx 2 \times n/\sigma$

no pipeline 1 per B, 1 per C, 2 codice

Agg. di A/D pipeline $\rightarrow 2 \times n/\sigma$
 invece fault comp. $\approx 4 \times n/\sigma + 2$

Agg. write-through $\approx 2 \times n/\sigma + 2$

$$T = t_{ok} + (4 \times n/\sigma + 2) \times T_{rep} + T_{write}$$

```
SUB R1, R1, R1
```

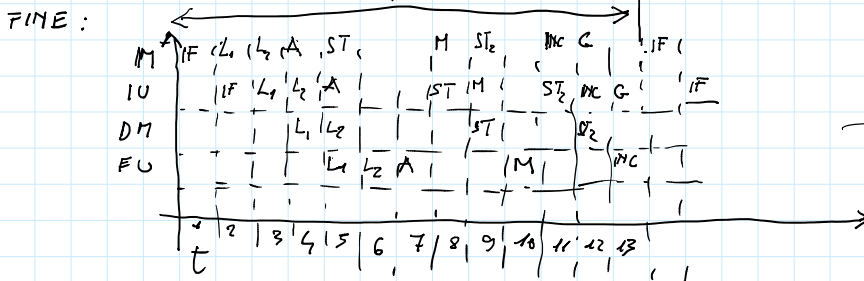
```

LOOP : IFG R1, RM, FINE
      LD1, RB, R1, Rb
      LD2, RC, R1, Rc
      1U-EU (ADD Rb, Rc, Rq)
      ST1, RA, R1, Rq
      1U-EU (MUL Rb, Rc, Rq)
      ST2, RD, R1, Rq
      INC R1
      GOTO LOOP
    
```

$$t_d = t_{ok} = 3 \times n \times t$$

tempo reale $13 \times n \times t$

$$Eff. \text{ unproc. } \rho = \frac{3}{13}$$



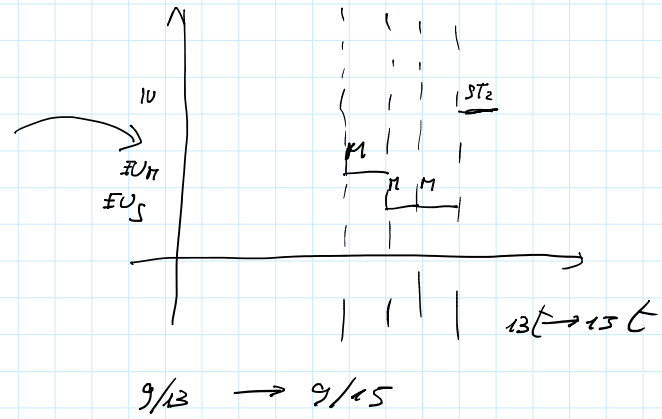
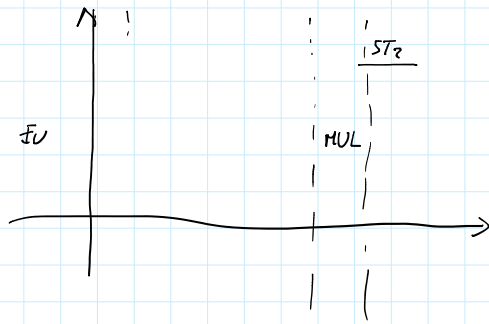
$9 \times n \times t$

$4 \times n \times t$

$$13 \times n \times t + \left[2 \times \left(\frac{n}{\sigma} \right) + 2 \right] T_{rep}$$

FU Pipeline

Master +/- VF, slave * VF ~ 2t

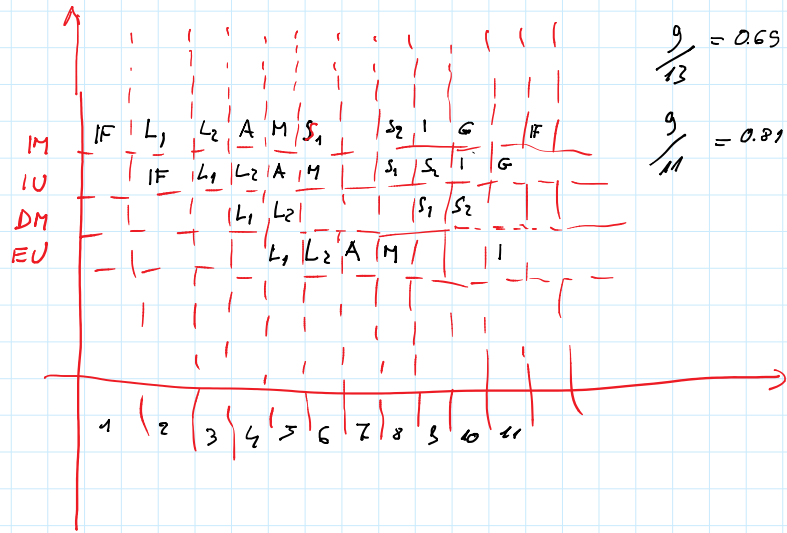


1^a opt. sul codice → aumento distanza delle dipendenze IU-EU

13 → 11

```

Loop: IF>
  { LD1
  { LD2
  { ADD
  { MUL
  { ST1
  { ST2
  INC
  QUIT
    
```



$$\frac{9}{13} = 0.69$$

$$\frac{9}{11} = 0.81$$

2^a att.

annullo dst + delayed branch

```

SUB Ri, Ri, Ri
DEC RD
DEC BA
    
```

} delayed branch

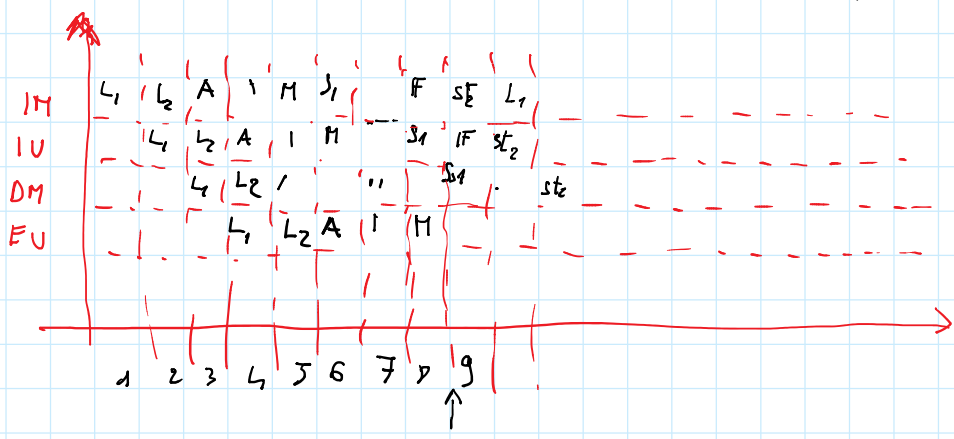
almeno 1 volta eseg.

eff 8/9 → 0.9

```

LOOP: L1
      L2
      ADD
      INC
      MUL
      ST1
      IF<
      ST2
    
```

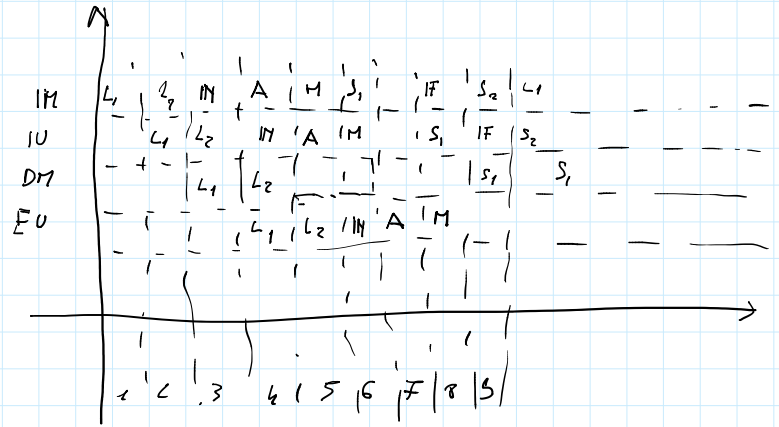
LOOP ← non si volta solo 1 volta alla fine



```

    LOOP: L1
           L2
           INC
           ADD
           MUL
           ST1
           IF
           ST2
    
```

Loop

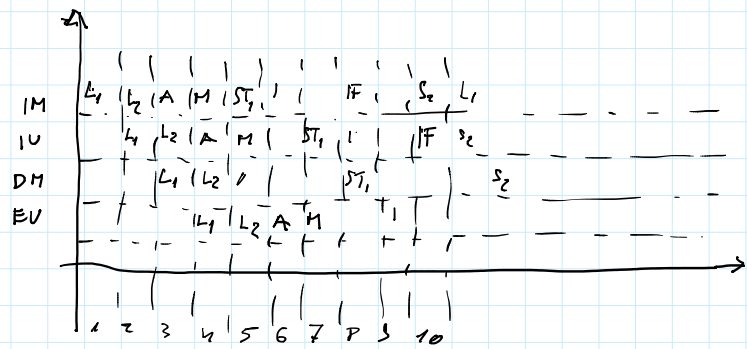


Permettono un'istanza
aumentata di INC

diminuisce per ADD

```

    SUB R1, P1, R1
    DFC RB
    LOOP: LD1
           LD2
           ADD
           MUL
           ST1
           INC
           IF
           ST2
    
```



for {i=d, i < N, i++}

$$A[i] = B[i] * c_1 + D[i] * c_2$$

$c_1, c_2, c_3 \Rightarrow$ costante nei reg. prima di andare nel loop

$$B[i] * D[i] + c_1 * c_2$$

$$D[i] = B[i] * A[i]$$

$$B[i] = D[i] * c_3 + Q[i]$$

exp 1

```

    LOOP: IF >= R1, RN, #INC
           LD1  RB, R1, RB
           LD2  RD, R1, RD
           MUL1 RB, R1, RT1
           MUL2 RD, R2, RT2
           ADD1 RT1, RT2, RT1
           ST1  RA, R1, RT1
           EXP1
           MUL3 RT1, RB, RT1
           ST2  RD, R1, RT1
           LD3  RQ, R1, RTQ
           EXP2
           MUL4 RT1, R3, RT1
           ADD2 RT1, R9, RT1
           ST3  RB, R1, RT1
           INC  R1
           GOTO LOOP
    
```

R1 = c1

```

    LOOP: LD1
           LD2
           LD3
           MUL1
           MUL2
           ADD1
           MUL3
           ADD2
           INC
           ST1
           ST2
           IF
           ST3
    
```

add

store e load

15 t