Homework 1

Premise. This homework is optional but warmly advised to check the understanding of the student lecture-by-lecture. It should be used to improve the student preparation during the course. All the answers must be properly and clearly explained.

Exercise 1. A system is composed of two processes $\Sigma = (P, Q)$. Process $P$ generates a stream of $10^6$ pairs $(A, B)$ where $A$ and $B$ are two arrays of size $M = 4K$ integers. The ideal service time of the process is $T_{id-P} = M^2\tau$. The second process $Q$ executes the following computation on each pair:

```c
Q:: int A[M], B[M], C[M]; input channel ch_in(1); output channel ch_out;
while true do
    receive(ch_in, (A,B));
    for i=0 to M-1 do
        C[i]=0;
    for j=0 to M-1 do
        C[i] = F(A[i], B[j], C[i]);
    send(ch_out, C);
```

Function $F$ is available as a library with average computation time $T_F = 10^5\tau$. The parameters of the inter-process communication cost model are $T_{setup} = 200\tau$ and $T_{transm} = 100\tau$. Analyze the system by focusing on the following points:

a) evaluate the ideal/effective service time, the ideal/effective processing bandwidth and the relative efficiency of process $Q$;

b) evaluate the ideal/effective service time, the ideal/effective processing bandwidth, the relative efficiency, the latency (per stream element) and the completion time of system $\Sigma$;

c) determine whether process $Q$ is a bottleneck or not, and in case evaluate its optimal parallelism degree.

In the analysis assume the following architectural specifications:

1. multiprocessor with $N = 32$ PEs and 32 shared memory macro-modules;
2. D-RISC CPU with mean service time per instruction equal to $4\tau$;
3. each PE has on-demand 32K primary cache (16K instruction cache + 16K data cache) with block size equal to 8 words;
4. the base memory access latency per cache block is equal to $L_{read-C1}(\sigma) = 320\tau$;
5. Assume that after an inter-process communication the target variable is written in main memory. Therefore, at the first access to each target variable’s block, the block must be read from the main memory;
6. the architecture provides a communicator processor per PE.

Exercise 2. A process $P$ receives a stream of integers (let $x$ be a generic input element) and encapsulates an integer variable $s$ initialized to one. For each input $x$ the process executes the following computation: $\text{while true do } \{\text{receive}(ch_{in}, x); y = x \cdot s; s = s + 1; \text{send}(ch_{out}, y)\}$. Explain whether this computation can be correctly parallelized as a farm.

Exercise 3. Explain the meaning of the following phrases, proving that both statements are true under proper additional specifications: a) “no object is shared by processes $P$ and $Q$”; b) “the communication channel descriptor is shared by $P$ and $Q$.”