Mark with a cross the correct answer. Only one answer is correct per question. The test is completely unofficial and it will not be used as part of the HPC exam.

**Name and Surname:** ____________________________, **student id:** ______________, **email:** ____________________________

1. The Arithmetic Logic Circuit is
   A. a combinational circuit
   B. a sequential circuit
   C. a combinational circuit equipped with registers for storing the operands
   D. a sequential circuit equipped with registers for storing the operands

2. In a clock cycle
   A. only one elementary micro-operation can be executed
   B. a potentially unlimited set of micro-operations can be executed
   C. some compatible micro-operations can be executed provided that the Operating Part of the unit has the necessary sequential circuits to execute them in parallel
   D. some compatible micro-operations can be executed provided that the Operating Part of the unit has the necessary combinational circuits to execute them in parallel

3. Firmware units
   A. must all have the same clock cycle
   B. execute one micro-program
   C. can be classified as units delegated to control the flow of micro-instructions (control parts) and units delegated to execute the micro-instructions (operating part)
   D. to be interconnected it is necessary to link the output of a register or of a circuit in the first unit to an input of a circuit/register in the second unit

4. Level-transition interfaces
   A. implement a synchronous communication at the firmware level
   B. implement the interconnections between logic gates in a combinational circuit
   C. it is the basic technology for implementing LLC sequential circuits
   D. implement an asynchronous communication at the firmware level

5. I/O interrupts
   A. can be received by a processor only when it executes an I/O receive primitive
   B. can be received only if the processor is not executing a system call
   C. are listened at the end of the interpretation of every assembler instruction
   D. cannot be listened if the processor is running an invisible sequence of memory accesses

6. Caches
   A. translate virtual memory addresses into physical ones through their TLB
   B. use a different technology with respect to RAMs
   C. may contain a subset of the cache lines present in main memory
   D. generate a fault (miss) in case the requested physical address is not present

7. The main memory
   A. can be on the same chip of the processor(s)
   B. answers to memory access requests exactly with the same latency
   C. contains all the virtual pages of the running programs
   D. contains only the virtual pages of the Operating System functionalities

8. A system call is triggered by
   A. an exception generated internally by the processor
B. I/O devices only
C. an I/O unit after the completion of an asynchronous task (e.g., a read from disk)
D. from the DMA unit after the completion of an asynchronous task (e.g., a read from disk)

9. A running process
   A. cannot be de-scheduled if it is running a system call
   B. cannot be preempted if the scheduler is not time-sharing
   C. remains in execution until it is de-scheduled by a timer interrupt
   D. is not suspended in case of a cache fault (miss)

10. In a superscalar processor
    A. the execution latency of assembler instructions is less than the clock cycle length
    B. each pipelined unit is able to process more instructions per clock cycle
    C. are designed in order to avoid data and branch hazards
    D. they cannot be effected by branch hazards

11. A process in the suspended state
    A. can be awakened by only an interrupt received by the processor where it was running
    B. can be awakened by an interrupt received by any processor
    C. can be awakened only by the handler of an I/O interrupt
    D. is always running a system call

12. A process executing a system call
    A. is de-scheduled and a kernel process is executed responsible for handling the system call execution
    B. goes in the suspended state
    C. executes a special instruction causing an exception to the processor
    D. executes a standard procedure in its logical addressing space

13. A virtual page is
    A. a partition of the logical addressing space of a process that is translated in a set of contiguous physical addresses of the main memory
    B. a set of contiguous cache lines
    C. a set of logical addresses utilized to access to firmware-invisible registers in the CPU
    D. a set of contiguous blocks of a file in a secondary device like a disk

14. In a uni-processor system
    A. memory accesses can be received only by last level of cache of the processor
    B. only one assembler instruction per clock cycle can be executed
    C. more threads can be executed in parallel in case of hardware multi-threading facilities
    D. interrupts cannot be masked for protection reasons