High Performance Computing
Solution of the Background Test (1st Attempt)

The correct answers are highlighted using a blue-colored bold font in the text.

1. A combinational logic circuit is
   A. the implementation at the hardware level of a finite state machine
   **B. the implementation at the hardware level of a pure function**
   C. a digital circuit composed of logic gates and memory registers
   D. a digital circuit able to generate synchronous clock signals

2. In a sequential logic circuit
   A. the output at any instant of time depends only on the input levels present at input terminals
   **B. the output at any instant of time depends on the input levels present at input terminals and on the history of the past input levels**
   C. the output at any instant of time depends on the input level of exactly one input terminal (from this the definition of sequential)
   D. the state is read sequentially at each variation of the input levels of the input terminals

3. A clock cycle is
   A. the average time interval between the generation of two timer interrupts in a time-sharing system
   **B. the fixed time interval between the generation of two clock pulses during which all the registers outputs are stable and cannot change**
   C. the time interval spent by the processor to complete the execution of an assembler instruction
   D. the precision of the circuit present in any computer system that maintains the time of the machine

4. The addressing space of a process is
   A. the set of all the possible physical addresses that the processor can generate during the execution of a given process
   **B. the set of all the possible logical addresses translated by the translation function of a process**
   C. the subset of the memory locations that can be accessed by a process during the execution
   D. the data that can be accessed by a process during the execution including disk files

5. Page faults are
   A. interrupts received by the processor when a file to be read by a process is not completely loaded in main memory
   B. interrupts received when the requested cache line is not present and it must be transferred from the main memory (or from disk)
   **C. exceptions generated to the processor when the accessed virtual memory page is not currently loaded in main memory**
   D. exceptions generated when a process tries to access a protected memory area for which it does not have the read/write permissions

6. The virtual memory is
   A. **the set of the code instructions and data structures that a process can access through logical addresses in its addressing space**
   B. a virtual abstraction of the physical memory which consists in the main memory and additionally of back storages like disks
   C. the memory hierarchy of a computer system including caches, main memory and disks
   D. the memory hierarchy at the previous point expect the processor’s caches

7. In case of a cache miss
   A. the running process is always de-scheduled by the operating system in order to wait for the cache block (cache line) transfer
   B. the running process may be eventually de-scheduled by the operating system only if the block (cache line) is not present in main memory (e.g., it must be transferred from a mass storage)
C. the block (cache line) will be transferred in cache from the main memory by the firmware without involving the operating system, thus transparently to the running process
D. the process generating the miss will be aborted by the operating system

8. Input-Output units are
   A. units in the motherboard able to receive input/output signals from devices
   B. a circuit in charge of enabling/disabling the communication with a peripheral device
   C. **firmware units able to interface peripheral devices with the CPU through interrupts**
   D. a firmware unit that receives interrupts from the caches or the main memory when some data must be written in a peripheral device like a disk

9. Interrupts are
   A. Synchronous messages sent by the CPU to the I/O units in order to start an I/O operation with a peripheral device
   B. Asynchronous messages sent to the CPU in case of unexpected events (e.g., an assembler instruction requests to use a logical address that cannot be correctly translated)
   C. Synchronous messages sent by an I/O unit to the CPU in order to notify the running process that a previously triggered operation with an external device is complete
   D. **Asynchronous messages sent by an I/O unit to the CPU in order to notify a suspended process that a previously triggered operation with an external device is complete**

12. A running process can be de-scheduled
   A. in any case when it executes a system call requesting an operating system functionality
   B. if the process executes a system call that needs to change the protection level of the CPU
   C. if a cache miss occurs during the execution of an assembler instruction
   D. **if a page fault occurs and the page must be loaded from a mass storage device (e.g., a disk)**

11. What is the Memory Mapped I/O technique at the firmware level
   A. is a technique to map in the virtual memory of a process the content of a file in the filesystem
   B. is a technique to map in the physical memory of the machine the content of a file
   C. **is a technique enabling the CPU-I/O communication by using LOADs and STOREs**
   D. is a technique to enable a I/O unit to access directly the main memory outside the CPU control

13. The Direct Memory Access (DMA) technique is used
   A. **to access directly the main memory by a I/O unit of the system**
   B. to access directly the main memory by the processor without involving the caches
   C. to access directly the main memory by the caches without involving the MMU unit
   D. to allow the processor to generate directly physical addresses that do not need to be translated by the MMU unit

14. A system call is
   A. a call to a privileged procedure written directly in assembler
   B. a call to a standard procedure that needs to be executed by a process of the operating system that works with the highest privileged level
   C. a call to a special procedure of the kernel executed by an operating system process after the triggering of a hardware exception that raises the privileged level of the CPU
   D. **a call to a special procedure of the kernel executed by the calling process after the triggering of a hardware exception that raises the privileged level of the CPU**

15. Why a cache is faster than the main memory?
   A. because it is smaller and the access time increases linearly with the capacity
   B. because a cache is based on a different technology than RAMs (random-access memories)
   C. **caches are based on Static-RAMs that are faster but less dense than Dynamic-RAMs**
   D. the main reason is that caches are on-chip and thus closer to the processor