Bringing Parallel Patterns out of the corner: the P³ARSEC Benchmark Suite

A Benchmark Suite for parallel patterns-based applications

Parallel Pattern design of 12 out of 13 PARSEC benchmark applications

Implementation with FastFlow and SkePU2 publicly available

Comparison over 3 different shared memory multicore architectures (Intel Xeon, Intel Xeon Phi, IBM Power 8) using different implementations

Detailed results and comparison with additional frameworks can be found in:

D. De Sensi, T. De Matteis, M. Torquati, G. Mencagli and M. Danelutto,
“Bringing Parallel Patterns out of the corner: the P³ARSEC Benchmark Suite”
Under Review in ACM Transactions on Architecture and Code Optimization

M. Danelutto, T. De Matteis, D. De Sensi, G. Mencagli, and M. Torquati,
“P³ARSEC: towards parallel patterns benchmarking”
in Proceedings of the 32nd annual ACM Symposium on Applied Computing (SAC 2017)

Software available at: http://github.com/paragroup/p3arsec
http://calvados.di.unipi.it/paragroup/
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