Network Monitoring on Multi cores with Algorithmic Skeletons

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Increasing number of applications on IP and increasing speed of network interfaces (100M → 1G → 10G)
Networking scenario

Increasing number of applications on IP and increasing speed of network interfaces (100M → 1G → 10G)

Increasing need for highly efficient network monitoring applications

- special purpose hw/sw solutions from vendors
e.g. Tilera multicores:
  - 64 to 100 cores per socket, cache only (private L1, local/shared L2, 4 external memory interfaces)
  - high speed network interfaces with direct cache packet injection

- or commodity processors with extremely efficient programming techniques
  - no unnecessary overheads with kernel interactions
  - no unnecessary overheads for synchronization
Processing scenario

- General purpose:
  - 6 to 8 full cores per socket
  - up to 64/128 threads per socket (Sun/Oracle T3/4)
  - 80 cores per socket already demonstrated (Intel Terascale prototype)
**Processing scenario**

- **General purpose:**
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    (Intel Terascale prototype)

- **Special purpose:**
  - O(100) cores in GPUs
  - only suitable to support (some) data parallel code
  - impressive speedup over general purpose multicores:
    comparable speedup on a 48 AMD Magny chorus and on a
    (quite old) nVidia GTX285
  - time spent to send (packet) data to / receive (record) data
    from GPUs impairs usage for network monitoring
Current tools

- “low level” programming tools (Pthreads)
  → full responsibilities on programmers
- “higher level” programming tools (OpenMP, OpenCL)
  → most responsibilities still on programmers
Current tools

- “low level” programming tools (Pthreads)
  → *full* responsibilities on programmers
- “higher level” programming tools (OpenMP, OpenCL)
  → *most* responsibilities still on programmers

Recognized need for actually **high** level tools:

*Architecting parallel software with design patterns, not just parallel programming languages. Our situation is similar to that found in other engineering disciplines where a new challenge emerges that requires a top-to-bottom rethinking of the entire engineering process;*

Asanovic et al. “A View of the Parallel Computing Landscape” CACM 2009
Parallel design patterns

- from sw engineering community
- introduced by Massingill, Mattson, Sanders in early 2000
  - “Patterns for parallel programming” Addison-Wesley 2004
- design patterns à la Gamma book
  - name, problem, solution, use cases, etc.
- define 4 pattern spaces (layered):
  concurrency, algorithms, implementation, mechanisms
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  concurrency, algorithms, implementation, mechanisms

Application programmers

- should learn pattern lesson
- and implement it as needed in their own applications
Algorithmic skeletons

Independently developed but strictly related to design patterns:

- from parallel programming community
- introduced by Cole in 1988 as
  - parametric, reusable parallelism exploitation patterns
  - directly exposed to programmers as language constructs/library calls
  - completely hiding the technicalities related to parallelism exploitation
- languages & libraries since the '90
  - P3L, Skil, ASSIST, Muesli, SkeTo, Mallba, Muskel, Skipper, FastFlow, ...
Algorithmic skeletons

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Application programmers

- instantiate existing skeletons
- to (safely and efficiently) build their parallel application
Main goal of this work

- exploit structured parallel programming techniques
- to support network monitoring
- on commodity hardware
**FastFlow**

Advanced programming framework

- targeting multicores
- minimizing synchronization latencies
- streaming support through skeletons
- expandable
- open source

**Applications & Problem Solving Environments**
Directly programmed applications and further abstractions targeting specific usage (e.g. accelerator & self-offloading)

**FastFlow**
- High-level programming
- Low-level programming
- Run-time support

**Composable parametric patterns of streaming networks**
Skeletons: Pipeline, farm, D&C, ...

**Arbitrary streaming networks**
Lock-free SPMC, MPSC, MPMC queues, non-determinism, cyclic networks

**Linear streaming networks**
Lock-free SPSC queues and threading model, Producer-Consumer paradigm

**Multi-core and many-core**
cc-UMA or cc-NUMA

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http://www.di.unipi.it
FastFlow: simple streaming networks

Single Producer Single Consumer (SPSC) queue

- uses results from the ’80s
- lock-free, wait-free
- no memory barriers for Total Store Order processor (e.g. Intel, AMD)
- single memory barrier for weaker memory consistency models (e.g. PowerPC)
- very low latency in communications
FastFlow: simple streaming networks

Other queues: SPMC MPSC MPSC

- one-to-many, many-to-one and many-to-many synchronization and data flow
- use an explicit arbiter thread
- providing lock-free and wait-free arbitrary data-flow graphs
- cyclic graphs (provably deadlock-free)
FastFlow: high level programming abstractions

Several “streaming” skeletons provided

- **farm**

\[
\ldots x_{i+1}, x_i, x_{i-1} \ldots \rightarrow SPMC \rightarrow MPSC \rightarrow \ldots f(x_{i+1}), f(x_i), f(x_{i-1}) \ldots
\]

- **pipeline**

\[
\ldots x_{i+1}, x_i, x_{i-1} \ldots \rightarrow f \rightarrow g \rightarrow \ldots g(f(x_{i+1})), g(f(x_i)), g(f(x_{i-1})) \ldots
\]

- **farm with feedback (divide & conquer)**

\[
\ldots x_j', x_{j+1} \ldots \rightarrow f \rightarrow \ldots f(x_{i+1}), f(x_j'), f(x_i), f(x_{i-1}) \ldots
\]
Sample code

```java
int main(int argc, char * argv[]) {
    ...
    ff_pipeline pipe;
    s1 = new PacketCaptureStage(Npackets);
    s2 = new PacketAnalysisStage(...);
    s3 = new PacketAnalysisStage(...);

    pipe.add_stage(s1);
    pipe.add_stage(s2);
    pipe.add_stage(s3);

    if (pipe.run_and_wait_end() < 0) {
        // handle error ...
    }
    return 0;
}
```
FastFlow results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Parameters</th>
<th>Skeleton used</th>
<th>Speedup / #cores</th>
</tr>
</thead>
<tbody>
<tr>
<td>Matrix Mult.</td>
<td>1024x1024</td>
<td>farm no collector</td>
<td>7.6 / 8</td>
</tr>
<tr>
<td>Quicksort</td>
<td>50M integers</td>
<td>D&amp;C</td>
<td>6.8 / 8</td>
</tr>
<tr>
<td>Fibonacci</td>
<td>Fib(50)</td>
<td>D&amp;C</td>
<td>9.21 / 8</td>
</tr>
</tbody>
</table>

**Table:** Microbenchmarks parallelized using FastFlow.

<table>
<thead>
<tr>
<th>Application</th>
<th>Skeleton used</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>YaDT-FF</td>
<td>D&amp;C</td>
<td>4.5-7.5 Speedup</td>
</tr>
<tr>
<td>StochKit-FF</td>
<td>farm</td>
<td>10-11 Scalabitily</td>
</tr>
<tr>
<td>SWPS3-FF</td>
<td>farm no collector</td>
<td>12.5-34.5 GCUPs</td>
</tr>
</tbody>
</table>

**Table:** Applications parallelized using FastFlow.
FastFlow results

![Graph showing speedup of FastFlow's worker threads]

- Ideal: 0.5us
- 0.5us
- 1us
- 5us

Assessed results

FastFlow
NetFlow

Network protocol to collect IP traffic information

- by Cisco
- de facto standard (→ IPFIX)
- works on flows: unidir sequence of packets with same source, dest and type of protocol
- generates records hosting:
  - version and sequence number, timestamps
  - layer 3 headers & routing info
**PF_RING**

Linux new type of network socket

- extremely efficient device to kernel ring packet copy
- exploits Linux NAPI interface (interrupts + polling)
- two operation modes
  - device to (multiple) kernel rings → supports packet directing to different applications
  - device to memory mapped kernel ring → zeroes copy time → but directs packets to one application only
Architectural design

Three different kind of parallel designs
  ▶ simple multiple design re-using sequential components
  ▶ explore different possibilities
  ▶ to match packet capture related constrains

General design:
  ▶ modular in the number of packet capture queues
    → one or more PF_RING queues
  ▶ modular in the number of threads processing incoming packets
    → stages in a pipeline: each stage processes part of the captured packets
    → more pipelines attached to different PF_RING
Base design

pipe: 1 PF_RING queue, 1 reader stage, n stages processing packets
**Base design**

pipe: 1 PF_RING queue, 1 reader stage, $n$ stages processing packets

- **RDR**
  - reads captured packets
  - groups them in messages
  - each packet directed to one stage through hash label
  - forwards messages through the pipeline

- **WRK**
  - reads a message (group of packets)
  - processes packets with proper (own) hash flag
  - on termination forwards resulting records
Variations

- PF_RING
- RDR
- WRK1
- Hash Table (part 1)
- ... (orphaned)
- WRKn
- Hash Table (part n)
Variations
Variations
Packet processing

- Basic network monitoring → very fine grain processing
  - extract simple data fields from packets

- More data processing needed for more evolved inspection strategies

- ffProbe:
  - experiments made with the finer grain processing functions
  → results improve with larger grain
  and with more stages / pipelines
# Experimental results (absolute)

<table>
<thead>
<tr>
<th>schema</th>
<th>Par. degree</th>
<th>Thr#</th>
<th>Mega PPS</th>
<th>Memory footprint</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 pipeline</td>
<td>Seq</td>
<td>1</td>
<td>3.76</td>
<td>50M</td>
</tr>
<tr>
<td>n workers</td>
<td>1R + 1W</td>
<td>2</td>
<td>6.45</td>
<td>94M</td>
</tr>
<tr>
<td></td>
<td>1R + 2W</td>
<td>3</td>
<td>8.42</td>
<td>78M</td>
</tr>
<tr>
<td>2 PF_RING</td>
<td>1R + 1W per pipe</td>
<td>4</td>
<td>10.150</td>
<td>64M</td>
</tr>
<tr>
<td>2 pipelines</td>
<td>1R + 2W per pipe</td>
<td>6</td>
<td>10.143</td>
<td>64M</td>
</tr>
<tr>
<td>2 PF_RING</td>
<td>2R + 1W</td>
<td>3</td>
<td>5.54</td>
<td>115M</td>
</tr>
<tr>
<td>1 pipeline</td>
<td>2R + 2W</td>
<td>4</td>
<td>9.13</td>
<td>150M</td>
</tr>
<tr>
<td></td>
<td>2R + 3W</td>
<td>5</td>
<td>10.033</td>
<td>150M</td>
</tr>
</tbody>
</table>

on a Dual Nehalem (Xeon E5520, 2.27GHz) with 10 Gbit Intel-based Silicom NICs

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http://www.di.unipi.it
Comparisons (nProbe)

A single instance does not scale with the thread number over 3Mpps:

Multiple instances on different PF_RING queues process as many packets as ffProbe:
Assessments

- High level, highly efficient parallel programming environment
  - supports network monitoring
  - on commodity hardware
  - targeting 10Gbps network interfaces
  - different parallel design experimented with negligible programming effort (once base sequential components have been defined)
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- High level, highly efficient parallel programming environment
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- High speed network monitoring
  - special purpose hw → commodity hw
  - systems (as tested) in the 3-4K euro range
Future (ongoing) work

To be improved:
- modularization of analysis code (plugin)
- ...

Product design currently on going:
- clean up and engineering of the code
- documentation (internal, user)
- experiments on larger core configurations
- to be released under open source license
Any questions?

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