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Power Modelling for Heterogeneous Cloud-Edge Data Centers

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Abstract. The research reported in this paper is focused towards developing next generation power modelling techniques that can automate and simplify power modelling for heterogeneous cloud-edge data centers. Our research firstly develops an automated hardware performance counter selection method that appropriately selects counters most correlated to power on both ARM and Intel processors. Secondly, we propose a noise filter based on clustering that can reduce the mean error in power models. Finally, we propose a two stage power model that surmounts challenges in using existing power models across multiple architectures. The key results are: (i) hardware performance counter selection is automated and simplified without sacrificing accuracy of power models, (ii) the noise filter reduces the mean error in power models by up to 55%, and (iii) the two stage power model can predict dynamic power with less than 8% error on both ARM and Intel processors, which is an improvement over classic power models.

Keywords. power modelling, cloud-edge computing, heterogeneous data centers, hardware counters, regression algorithms

1. Introduction

It is anticipated that resources of future data centers will span across both what is known today as the cloud and the edge of the network [4]. In such an environment, applications will be distributed across data center processors, for example Intel Xeon processors, and low power processors, such as ARM popularly employed in embedded systems located on nodes at the edge of the network [6]. Power modelling of processors in this context will play a key role in maintaining the stability of the computing environment [2].

A large proportion of existing power models rely on multiple hardware activities of the processor represented by hardware performance counters, referred to as hardware counters for estimating power [3]. The hardware counters necessary to build accurate power models substantially differs across different processors due to the differences in the instruction set, pipeline, cache architecture and on-chip interconnect. The hardware counters are usually selected manually on the basis of experimental knowledge of the processor [1]. Typically, all possible hardware counters that can be obtained from a processor are extensively explored using a cumbersome trial and error approach after which a suitable few are selected [5]. Such an approach will not scale for multiple processor

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