

Bridging the Gap between Software and Hardware Designers

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Abstract

Modern Systems-on-Chip (SoC) architectures and CPU+FPGA computing platforms are moving towards heterogeneous systems featuring an increasing number of hardware accelerators. These specialized components can deliver energy-efficient high performance, but their memory subsystem is usually responsible for most of the area and power dissipation. Therefore, it is crucial to understand how to design and optimize such components to implement the desired functionality. In this talk, I will present and discuss the current challenges for accelerating an application in hardware. I will also present a complete system-level methodology to address most of the issues for the generation of accelerators with specialized and multi-bank memories. This methodology combines high-level synthesis methods for the synthesis of the functionality and prototype CAD tools for the optimization of the memory subsystem. This combined solution generates accelerators directly from unmodified C code, including several technology-aware optimizations to reduce the memory cost (area and power) by efficiently reusing the physical banks for storing different data.