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Modeling technique and a simulation tool for analysis of clock synchronization in communication networks

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Clock Synchronization

- Clock synchronization is introduced as a tool to control the coordination of complex systems
- Many common use network applications and protocols depend on a sufficiently accurate synchronization (e.g. NFS)
- Electromechanical devices and robots need a common time reference
- Communication networks require frequency synchronization to control number of slips

Standardization efforts

- For Telecom synchronization requirements are specified by ITU-T G.810-824, ETSI EN 300 421 and other standards
- The NTP is the most successful clock synchronization protocol (accuracy with current network technology worse than 1msec)
- The IEEE 1588 is an emerging standard that targets advanced telecom environments, industrial automation, robotics, military and other environments, with accuracies below 1µsec.

Master-Slave architecture

- General reference architecture distinguishes Master and Slave clocks
- Each Master can feed one or more Slaves with a reference clock signal
- Such clock signal can be in the form of timestamped messages, T1/E1 or SONET/SDH line rate signals
- One Slave can accept input from several Masters, in order to improve accuracy and robustness

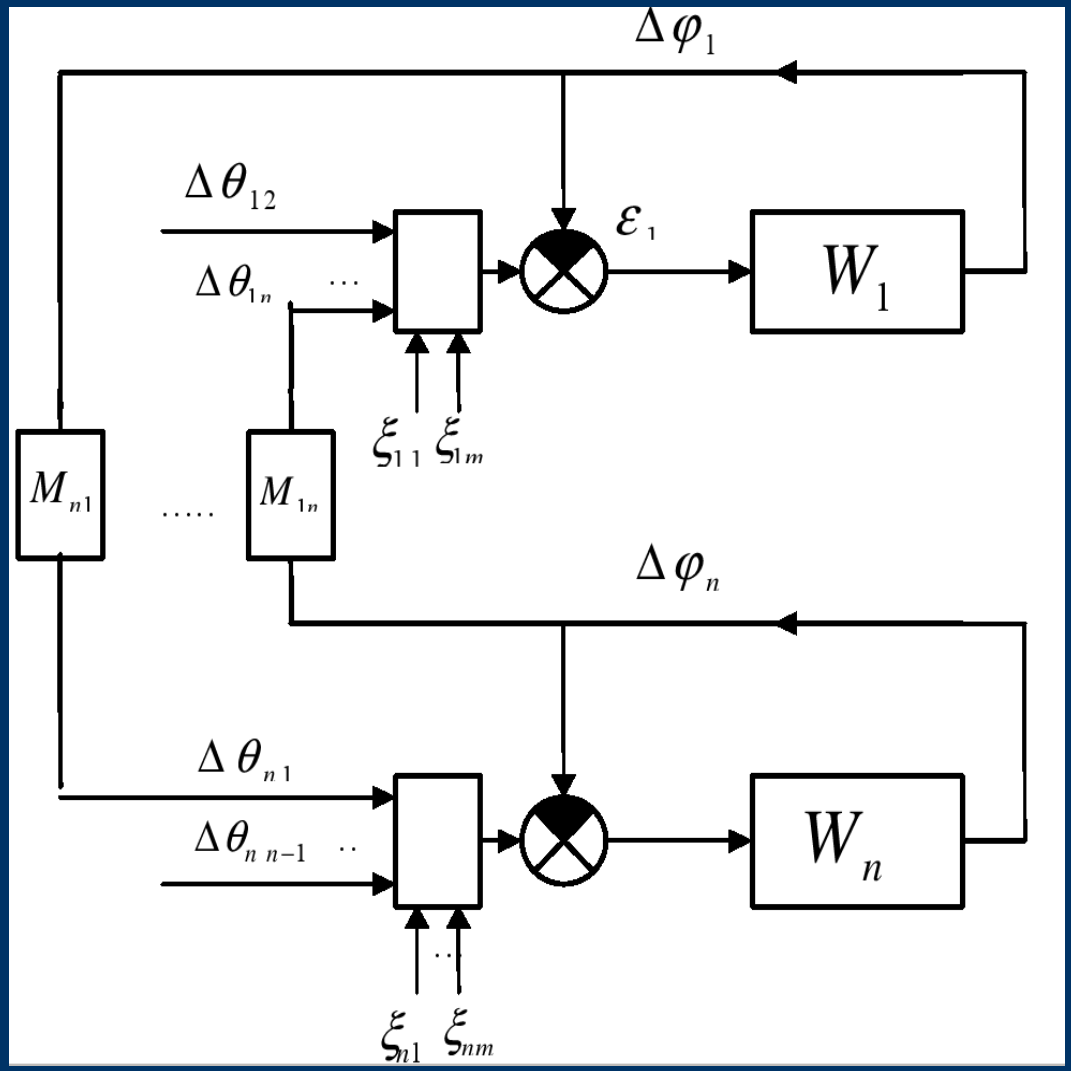
Clock synchronization issues

- The performance of the transmission line carrying the clock signal is variable
- The Master Clock is characterized by a bounded stability and internal phase noise
- The Clock Control device inside the Slave is characterized by a bounded stability and noise
- Standard performance criterion for Telecom:
  - Maximum Time Interval Error (MTIE)
  - Relative Time Interval Error (RTIE)
  - Time Deviation (TDEV)

Simulation and Analysis

- The dynamics of a system composed of interconnected masters and slaves are quite complex
- A simulation tool helps to anticipate their behavior in order to evaluate design options
- Building blocks:
  - Slave Clock model
  - Master Clock model
  - Synchronization Link model
  - Connectivity matrix

Model block diagram



- Clock deviations are transferred among boxes
- M boxes represent links
- W boxes represent PLL clocks
- Clocks from different sources are combined

Simulation technique

- The continuous transfer function

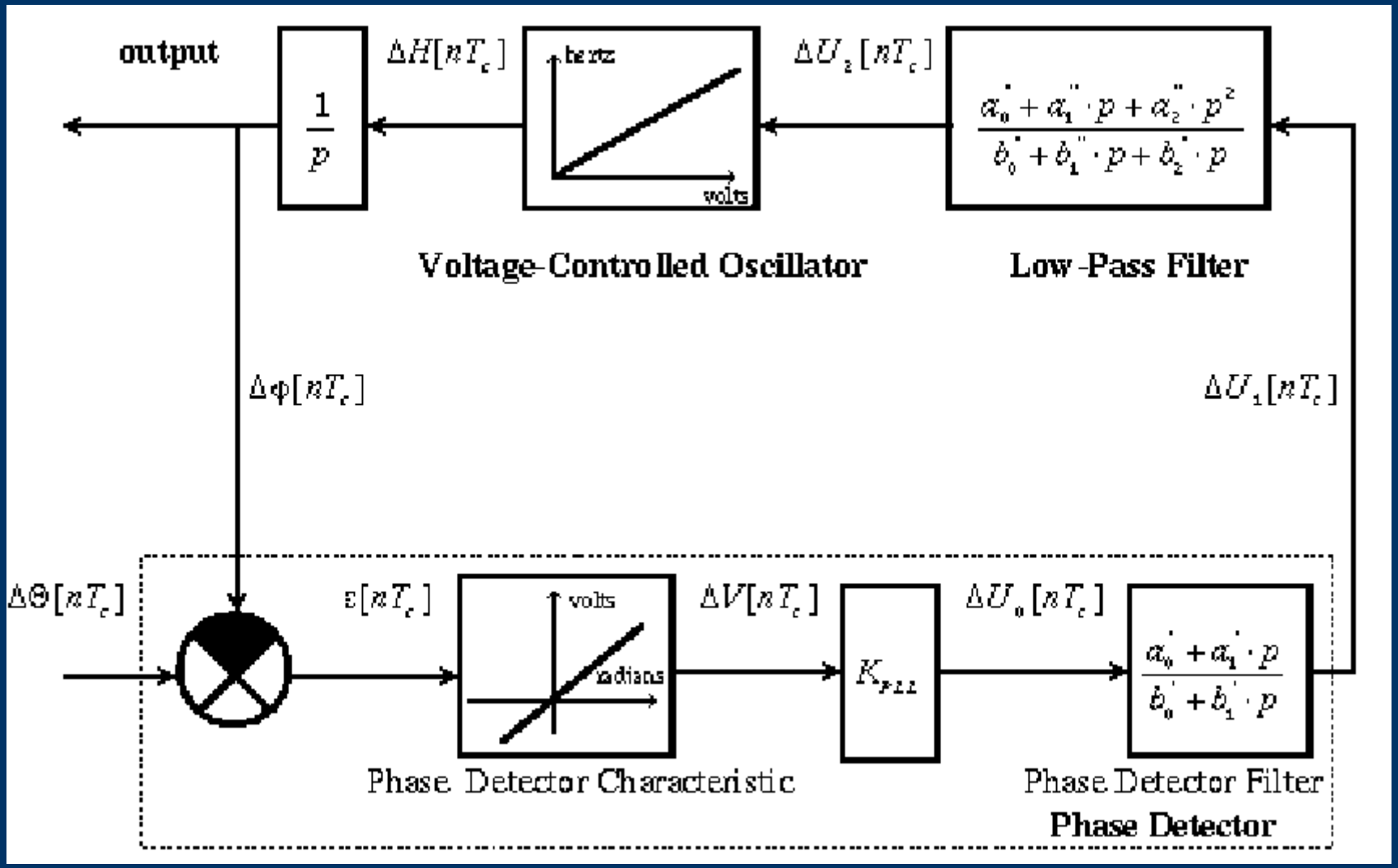
$$W(p)=\frac{a_0+a_1\cdot p+a_2\cdot p^2+\ldots+a_k\cdot p^k}{b_o+b_1\cdot p+b_2\cdot p^2+\ldots+b_k\cdot p^k}$$

is transformed into a discrete domain using Boxer-Thaler

$$Y[nT_c]=\frac{1}{B_k}\left\{\sum_{\nu=0}^{k}A_{k-\gamma}\cdot X[nT_c-\nu T_c]-\sum_{\nu=1}^{k}B_{k-\gamma}\cdot Y[nT_c-\nu T_c]\right\}$$

- S-matrices simplify the computation of A and B coefficients.

Building blocks: the slave

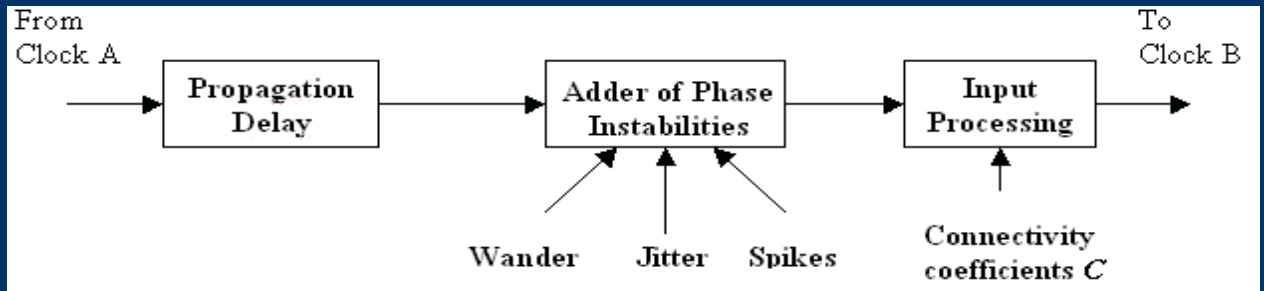


Building blocks: the master

$$o_1[nT_c] = o_{st}[nT_c] + o_{ac}[nT_c] = o_1[nT_c - T_c] + \frac{T_{sim}}{T_c} \cdot 2\pi \cdot (r_{st}[nT_c] + r_{ac}[nT_c])$$

- Bounded systematic frequency variation.
- Inaccuracy adding Gaussian white noise.

Building blocks: the link



$$\Delta\Theta_{\sum}[n] = \Delta\Theta_{wander}[n] + \Delta\Theta_{jitter}[n] + \Delta\Theta_{spikes}[n]$$

$$\Delta\Theta_{wander}[n] = \sum_{i=1}^{m} k_i \cdot \Delta t_i \cdot L_i \cdot \sin(2\pi \cdot F \cdot n + \varphi_0)$$

$$\Delta\Theta_{jitter}[n] = \sin(2 \cdot \pi \cdot f_{jitter} \cdot n)$$

$$\Delta\Theta_{spikes}[n] = \begin{cases} (-1)^{\mu} \cdot 2\pi \cdot \alpha, & n = m \cdot T \\ 0, & n \neq m \cdot T \end{cases}$$

- Interconnections between masters and slaves
- Jitter and diurnal wander affect clock transmission
- Random phase transients

Building blocks: the link

$$M(p) = \frac{Y(p)}{X(p)} = e^{-p\tau} .$$

$$\Delta\varphi^{\#}[n] = \frac{1}{B_1^{\#}} \cdot \left\{ A_1^{\#} \cdot \Delta\varphi[n] + A_0^{\#} \cdot \Delta\varphi[n-1] - B_0^{\#} \cdot \Delta\varphi^{\#}[n-1] \right\}$$

$$A_0^{\#} = 1 - \frac{2\tau}{T}, \quad A_1^{\#} = 1 + \frac{2\tau}{T}, \quad B_0^{\#} = B_1^{\#} = 1$$

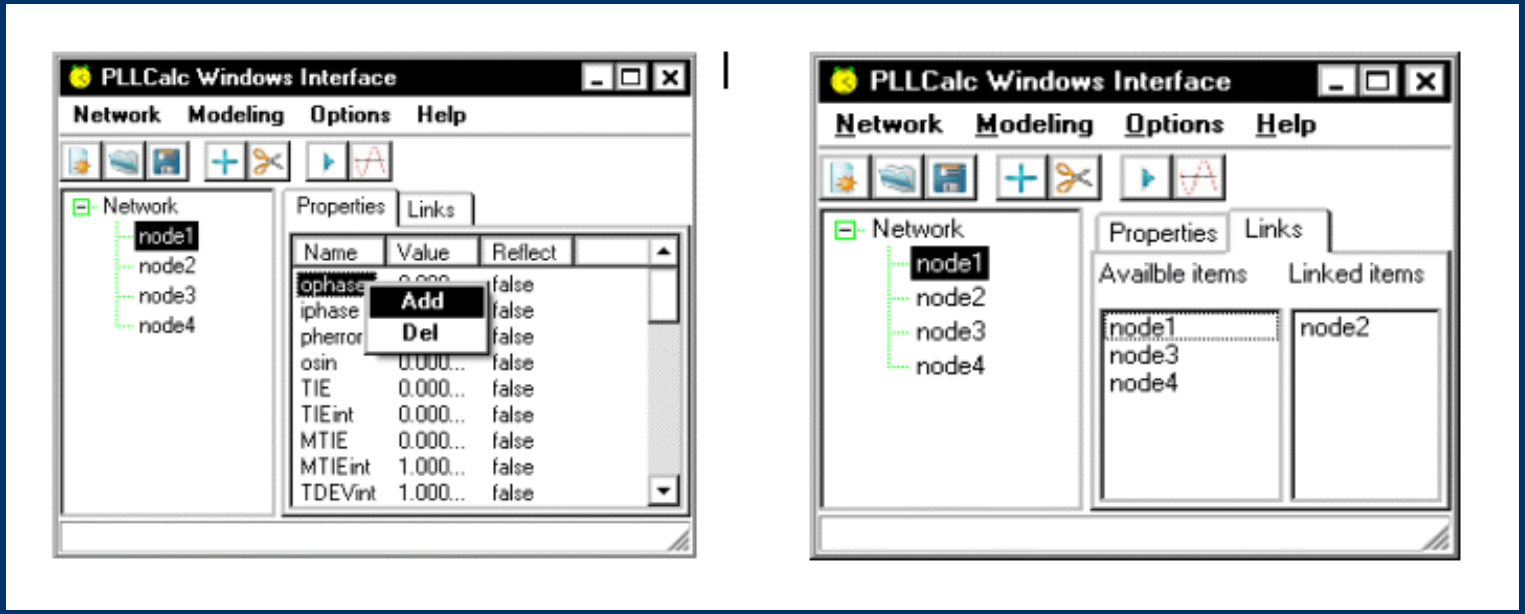
- The link is modeled with a constant delay
- Simplified trasnform, with coefficients

Building blocks: the C matrix

- Built into Input signal processing block
- Weighting reflects quality of inputs
- Supports single or multiple inputs
- Allows fault protection switching between input sources

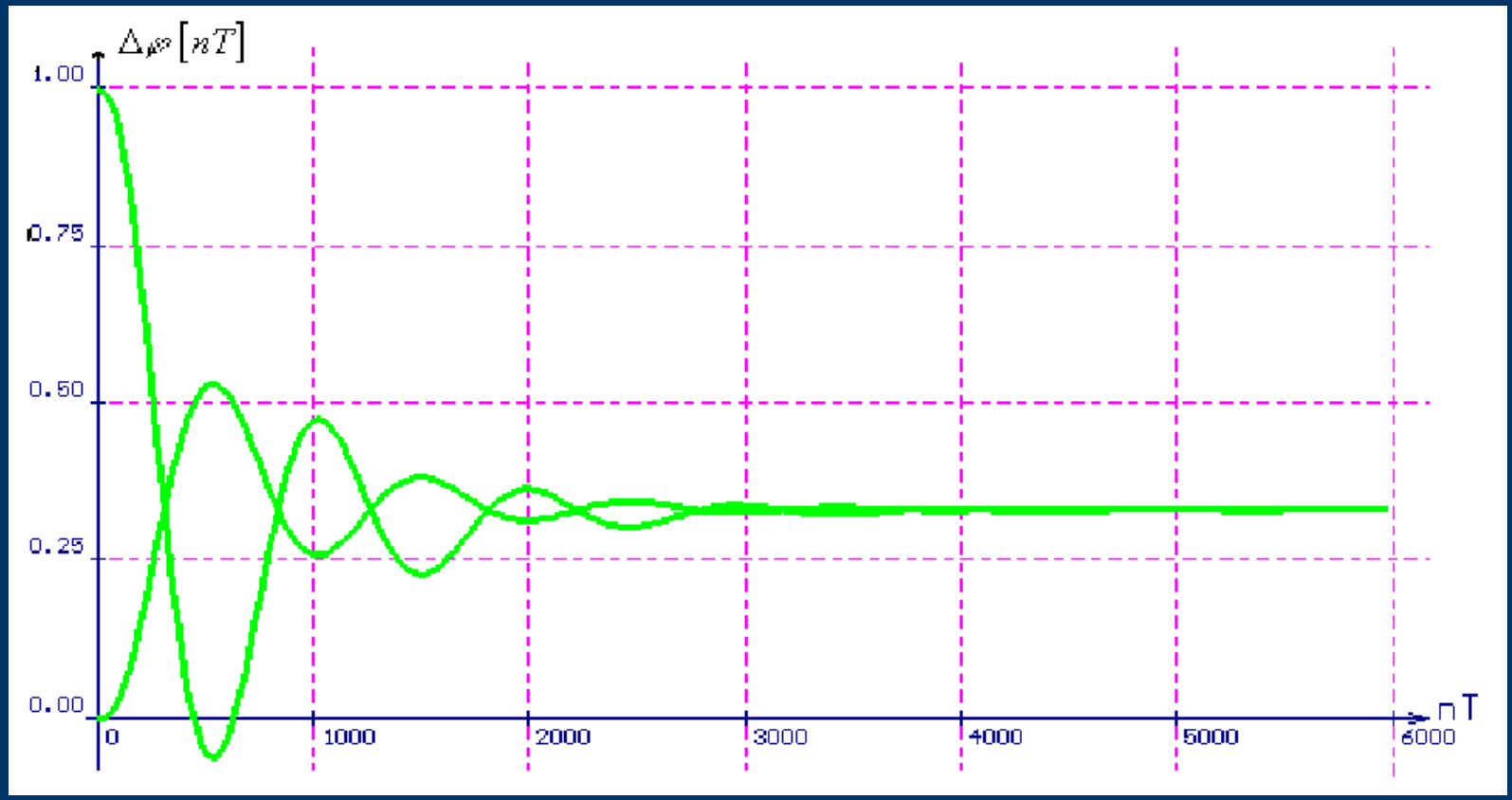
$$C = \begin{bmatrix} 0 & c_{12} & c_{13} & \cdots & c_{1n} \\ c_{21} & 0 & c_{23} & \cdots & c_{2n} \\ c_{31} & c_{32} & 0 & \cdots & c_{3n} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ c_{n1} & c_{n2} & c_{n3} & \cdots & 0 \end{bmatrix}$$

Simulation tool



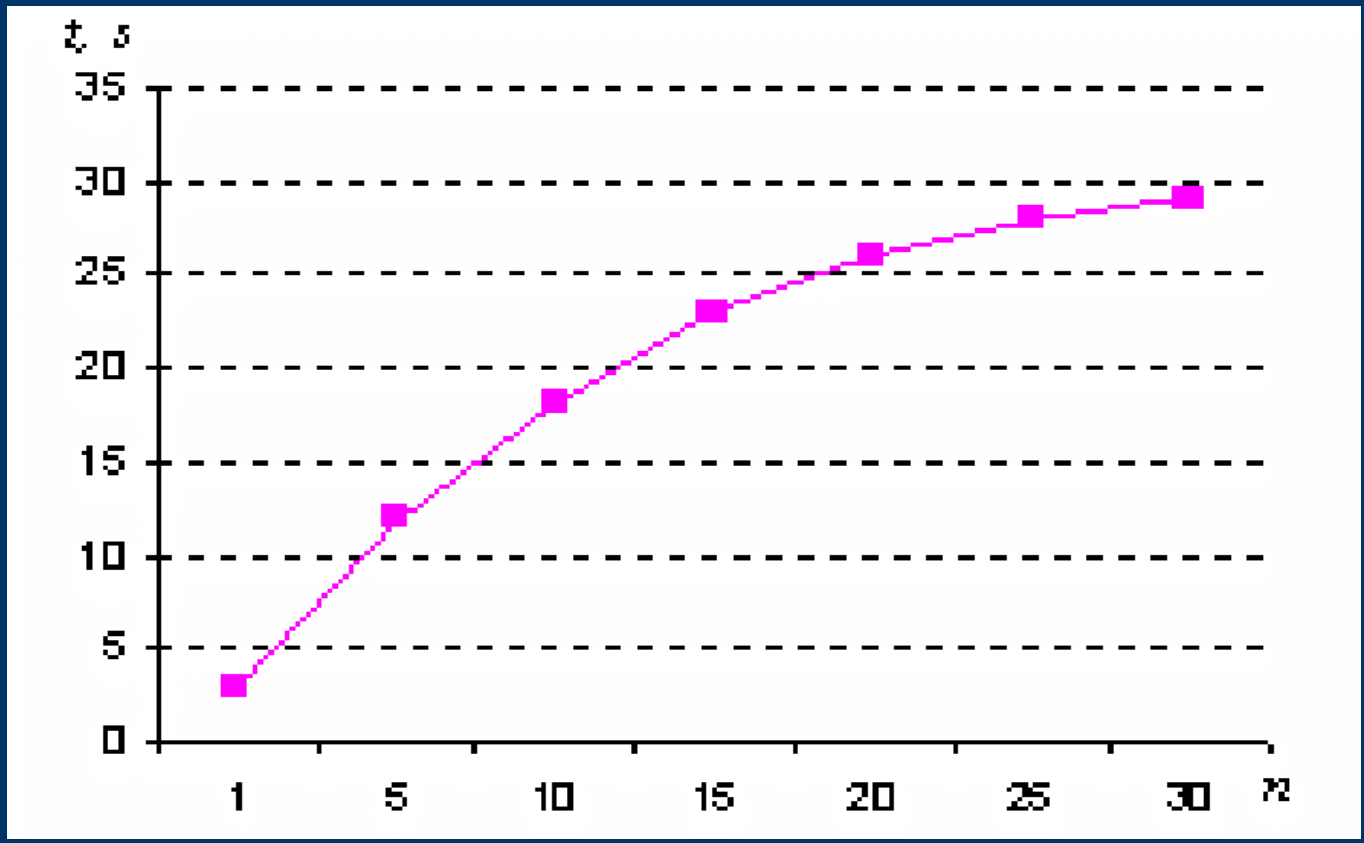
- Select parameters for clocks, links, input signals
- Create the desired network topology
- Choose the type of analysis and output parameters
- MS Windows environment, ANSI C++ and XML

Simulation results: convergence



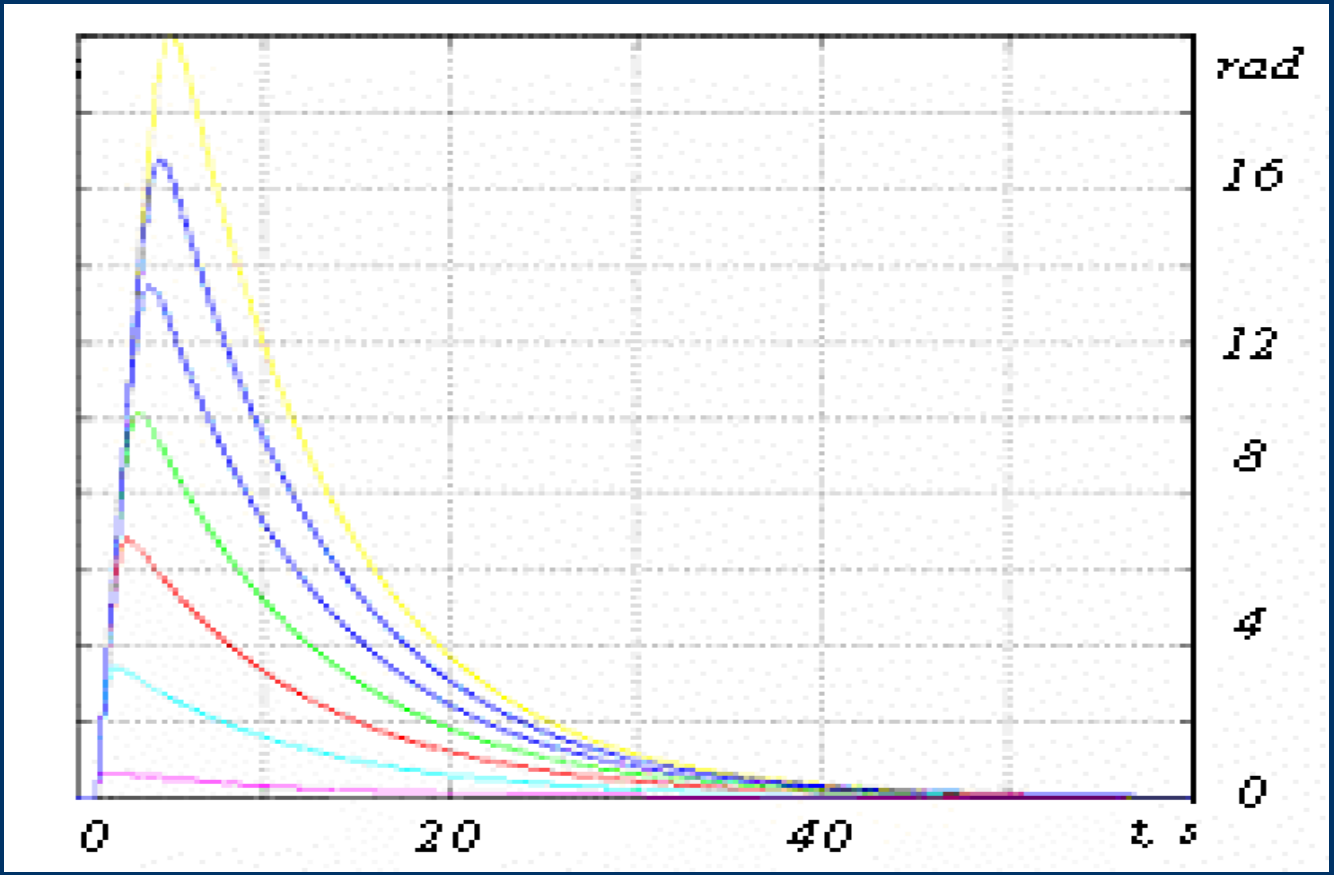
- Two clocks in a stabilizing arrangement converge

Simulation results: scaling



- Time to converge for systems of *n* nodes

Simulation results: diffusion

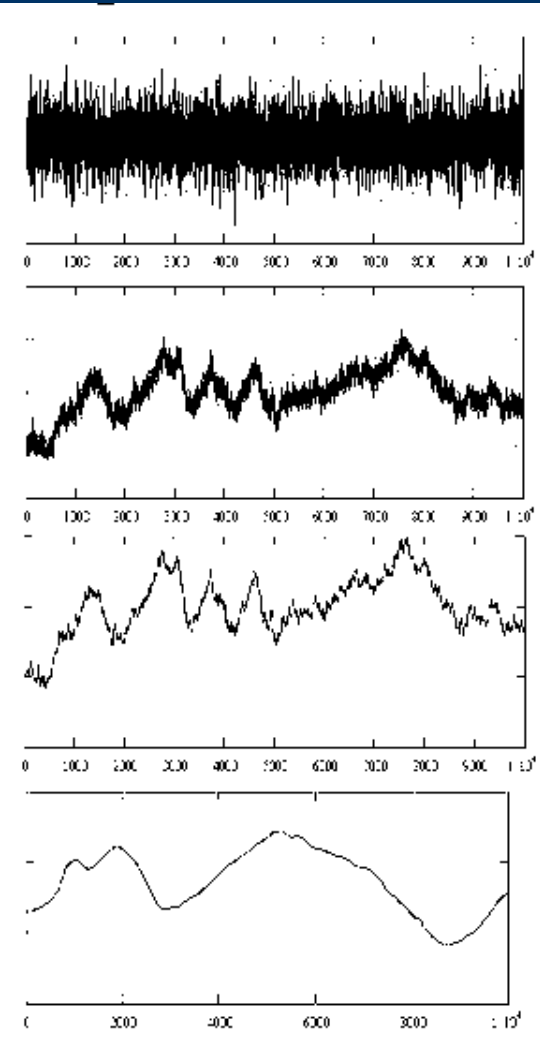


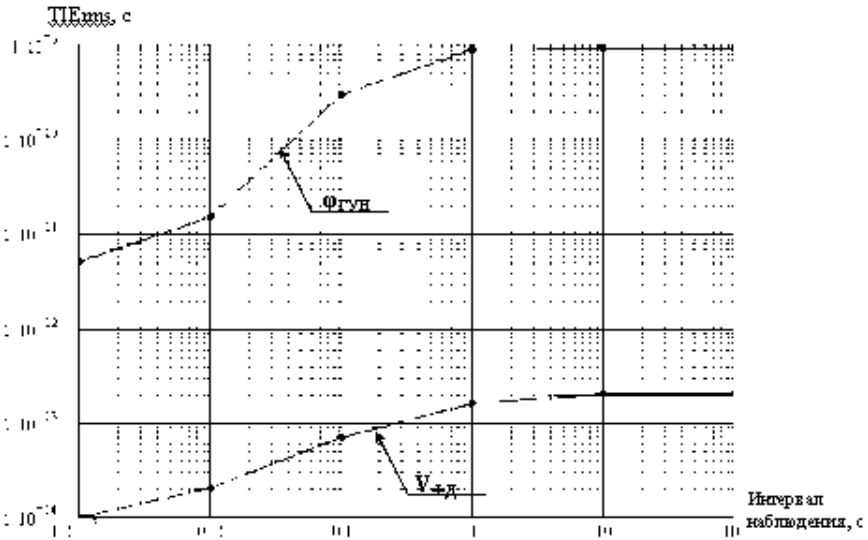
- Diffusion of a frequency jump in a chain of clocks

Conclusion

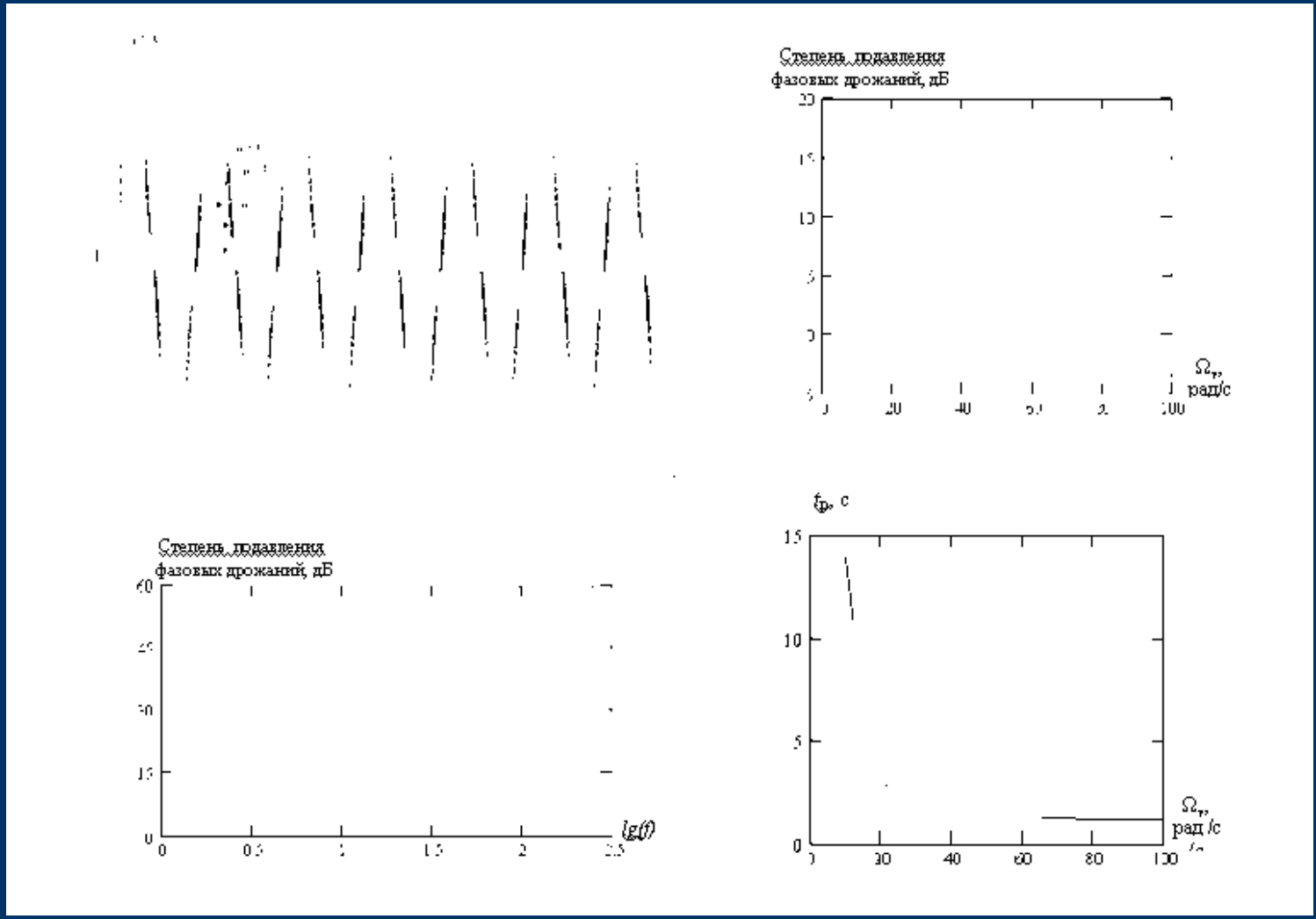
- The tool is easy to use, targeted to a specific problem
- It is significantly faster than using a general purpose mathematical tool
- Already used in production environments
- A modular structure allows the development of new features

Results: Analysis of slave clock noise

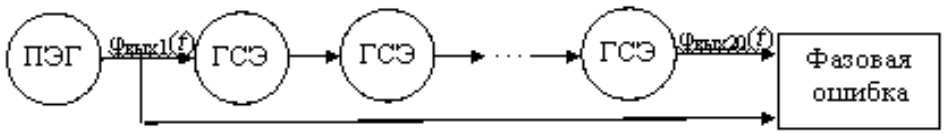


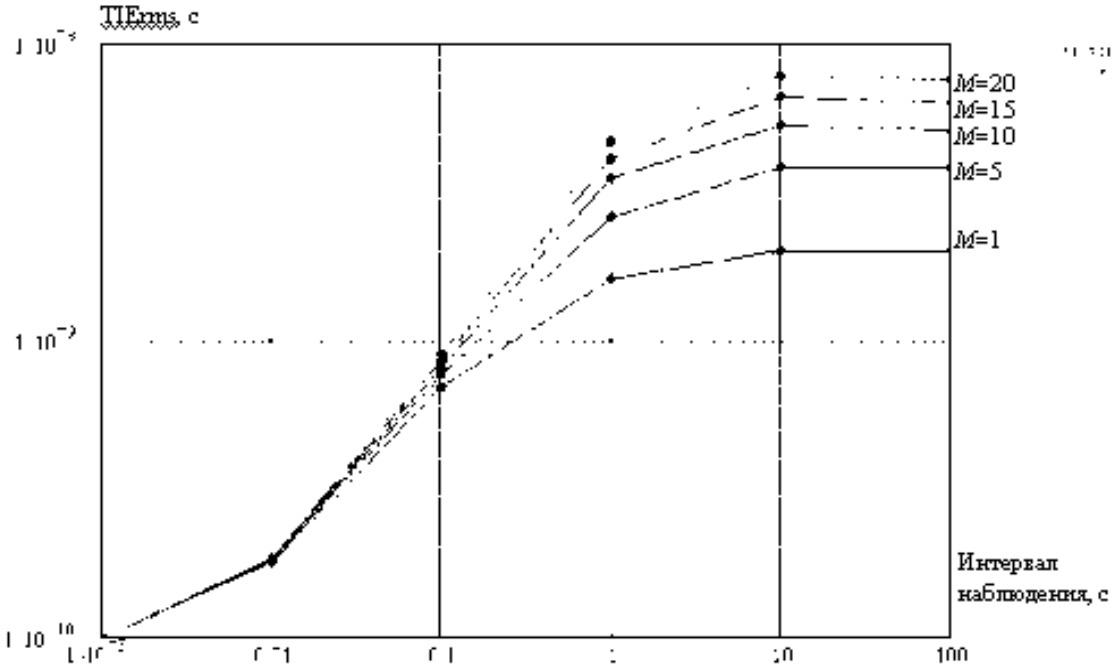


Results: Jitter analysis



Results: Noise accumulation





Results: Protection switching